A 170-260 GHz SiGe Frequency Doubler with 5-dBm Output Power and 13-dB Input Power Range

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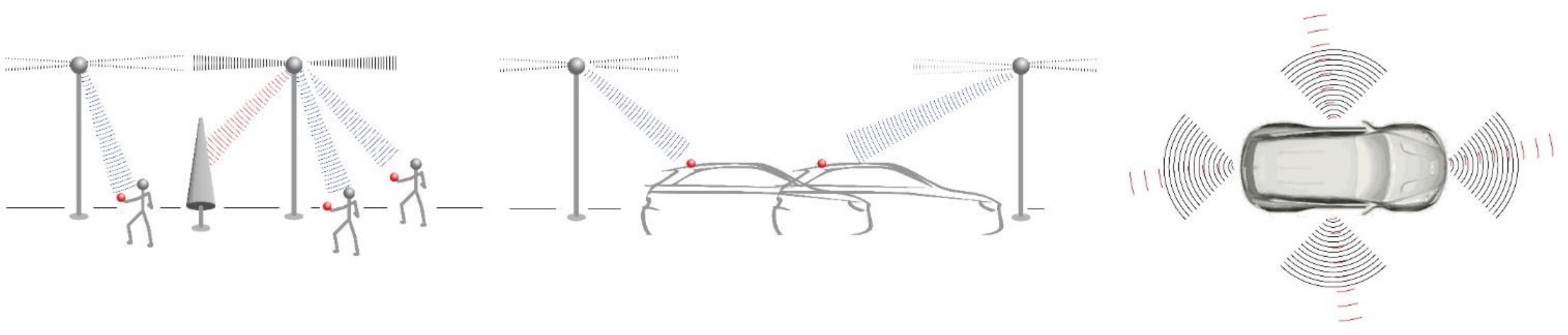
UC SANTA BARBARA

Motivation

- Power budget prohibitive for mobile transmit/receive systems above 100 GHz, 6G
- Reduce power through
  - Use of different semiconductors, heterogenous integration
  - Architectural optimization in array scaling to target a different SNR
  - Circuit techniques



Power Estimate: P. Skrimponis *et al.*, "Power Consumption Analysis for Mobile MmWave and Sub-THz Receivers," in *2020 2nd 6G Wireless Summit (6G SUMMIT)*, Mar. 2020, pp. 1–5. doi: 10.1109/6GSUMMIT49458.2020.9083793.

Motivation

- LO power dominates system power consumption
- Conventional frequency multipliers are driven at maximum with a single saturating power
  - Permanently sets performance for an architecture
- Want dynamic trade-off between LO power requirement and system performance for highly dynamic wireless channels
  - **Want a frequency multiplier that can handle a range of LO input powers**

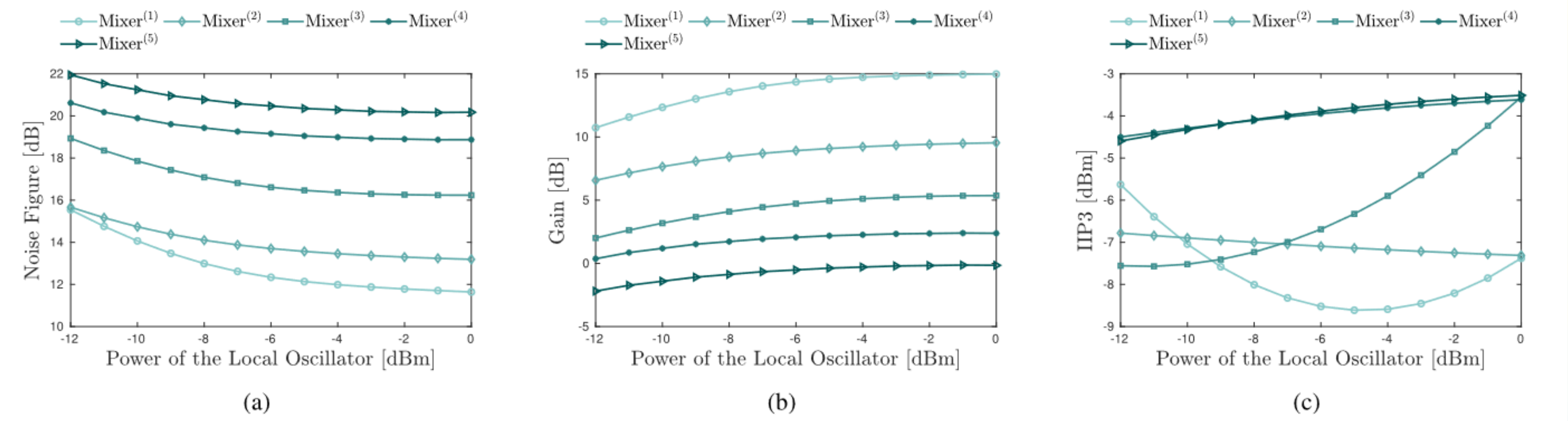
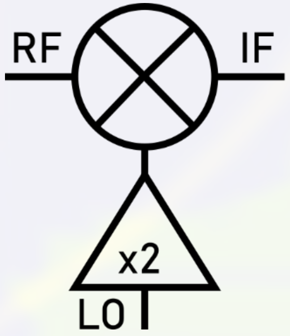


FIGURE 3. **Parameters of the IF mixers used in our analysis. We show noise figure in dB (a), gain in dB (b) and IIP3 in dBm (c) as a function of the input LO power.**

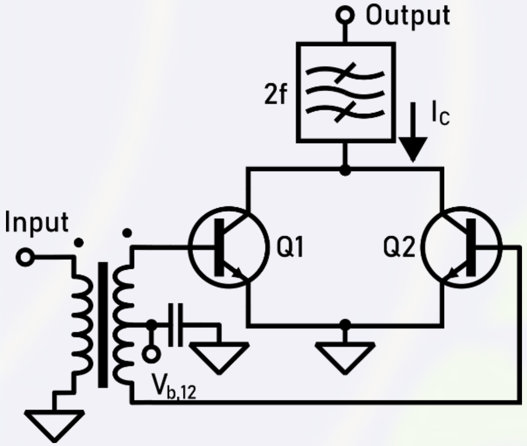


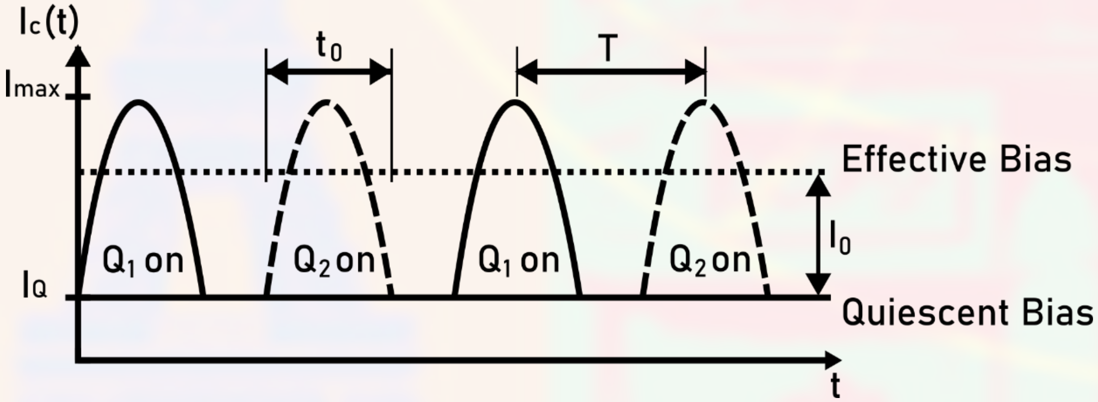
Architectural Optimization: P. Skrimponis *et al.*, “Towards Energy Efficient Mobile Wireless Receivers Above 100 GHz,” *IEEE Access*, vol. 9, pp. 20704–20716, 2021, doi: 10.1109/ACCESS.2020.3044849.

Push-pull Frequency Doublers

- Input signal is rectified to produce an output waveform
- Fourier series of output current:
  - ✅ Output contains even harmonics (desired)
  - **Output also contains an additional DC current I_0**
    - ☠️ **Affects biasing and gain**

Conventional Doubler



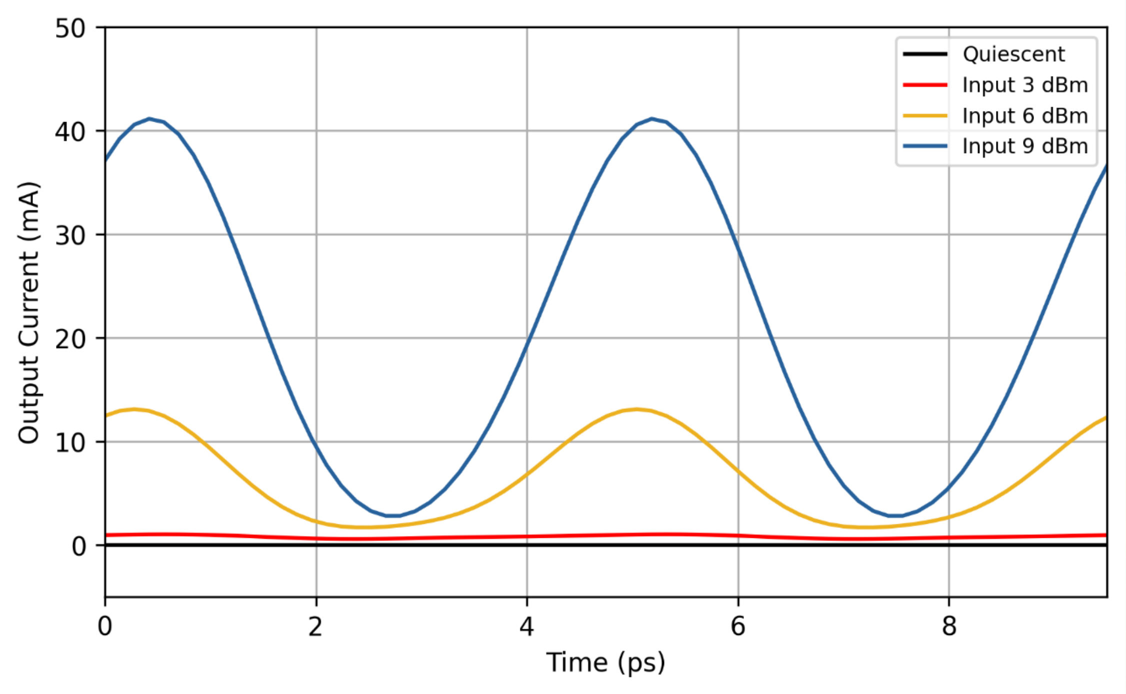


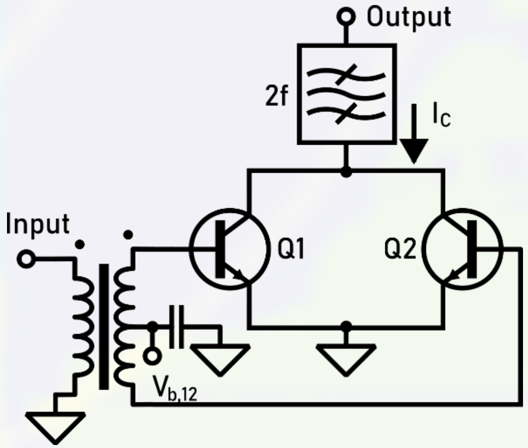
$$I_c(t) = I_0 + I_1 cos(\omega t) + I_2 cos(2\omega t) + \ \dots \ I_n cos(n\omega t)$$

$$I_n = I_{max} \frac{4t_0}{\pi T} \begin{cases} 1 & , \text{if } n = 0 \\ 2 \cdot \left| \frac{\cos\left(\frac{n\pi t_0}{T}\right)}{1 - \left(\frac{n\pi t_0}{T}\right)^2} \right| & , \text{if } n \text{ even} \\ 0 & , \text{if } n \text{ odd} \end{cases}$$

Effect of Output on DC Bias

- Output waveform adds DC bias current by I_0
- Transistor loses current density and gain at lower powers
  - Change bias to compensate?

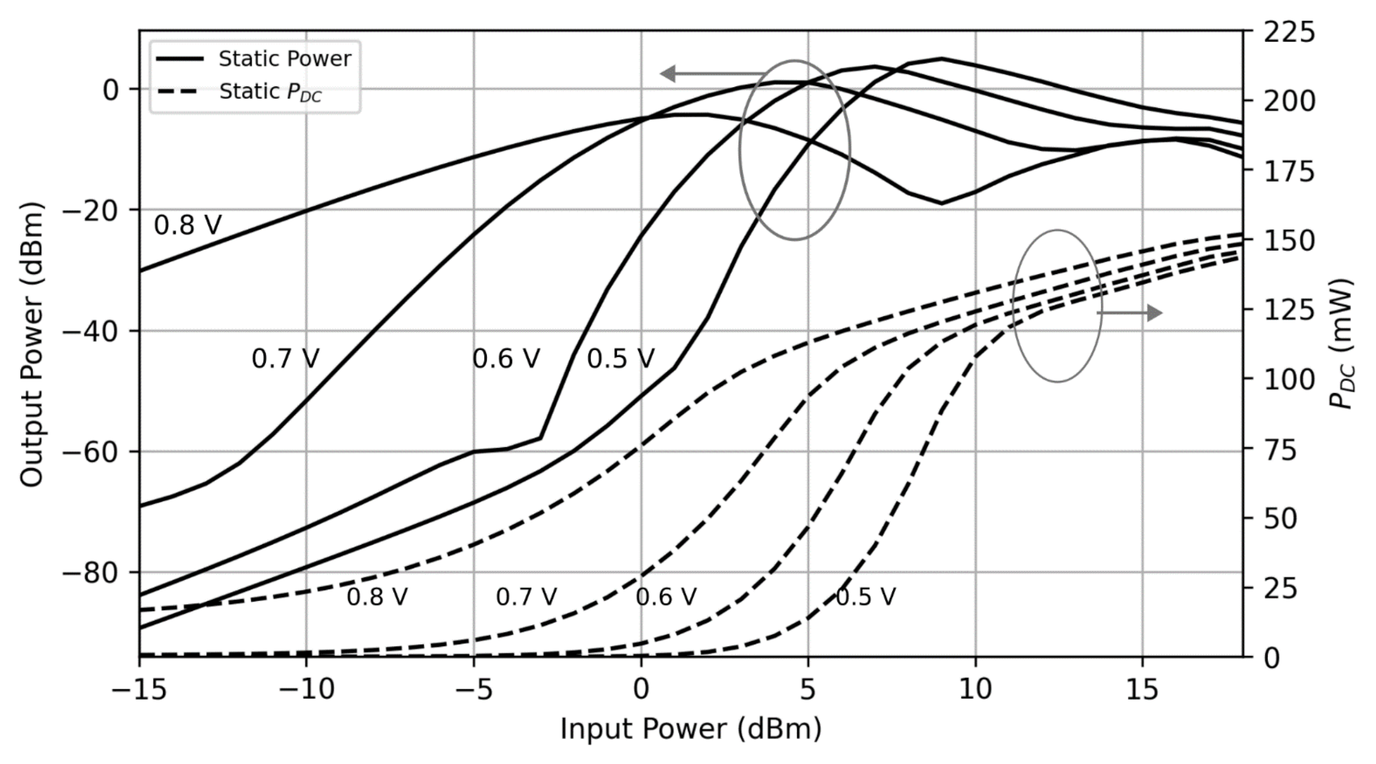


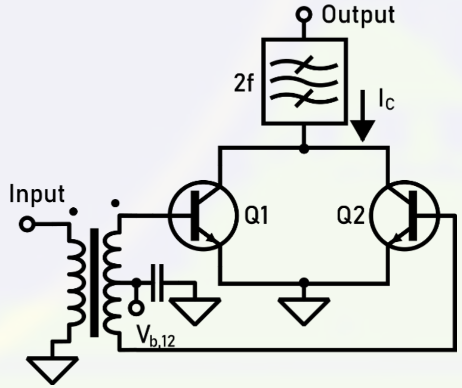


Simulated (Transistors only, no filtering)

Simulated Effect of Static Biasing

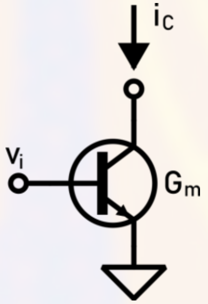
- Requires a choice of bias
- ☠️ High gain sensitivity to input power





Problem: Additional DC Current I_0

- DC current sensitivity results in non-linear gain
  - Extreme sensitivity to input power



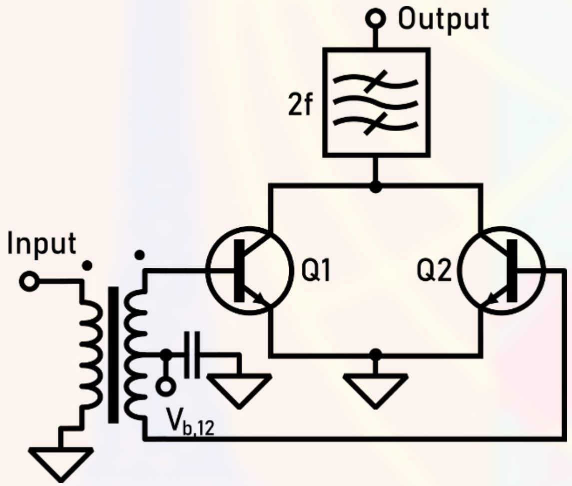
$$i_C = G_m(I_0 + I_Q)v_i$$

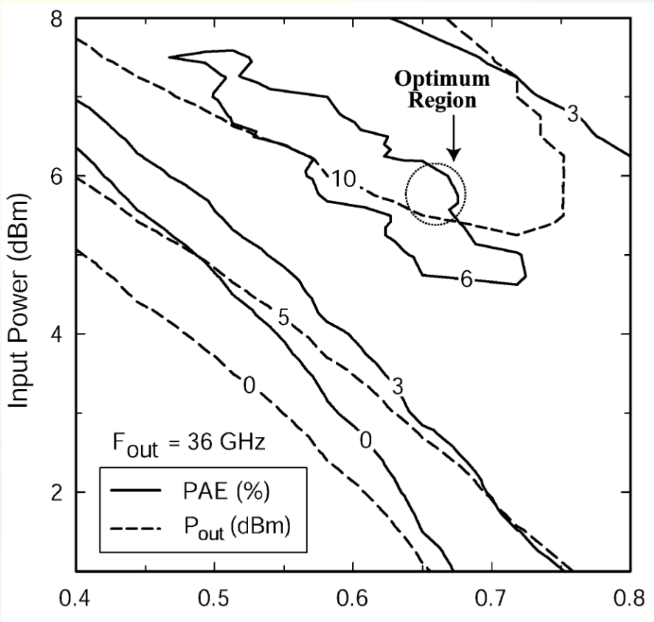
$$I_0 = \frac{4t_0}{\pi T} i_C = \frac{4t_0}{\pi T} G_m(I_Q + I_0)v_i$$

- Solutions:
  - Operate at a single saturating LO power or
  - **Enforce current density to eliminate additional DC current I_0**

Conventional Approaches

Static Bias Approach



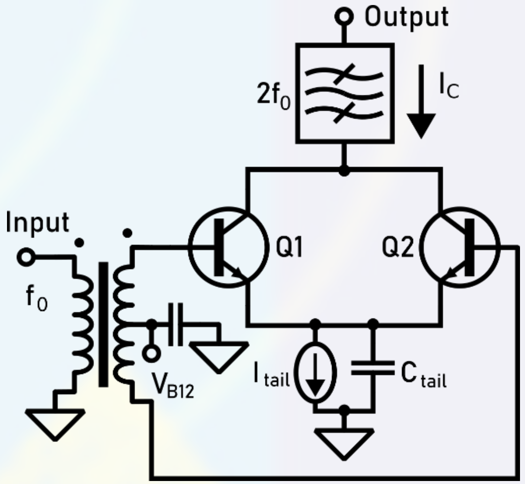


[Hung 2005]

- Set an optimum input bias V_{B12} for an input power
- ☠️ No bias enforcement
- ☠️ Gain changes with input power (high sensitivity)
- ☠️ Limited output power when voltage is tuned for a lower input power

J.-J. Hung, T. M. Hancock, and G. M. Rebeiz, "High-power high-efficiency SiGe Ku- and Ka-band balanced frequency doublers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 2, pp. 754–761, Feb. 2005, doi: 10.1109/TMTT.2004.840615.

Current Tail Approach

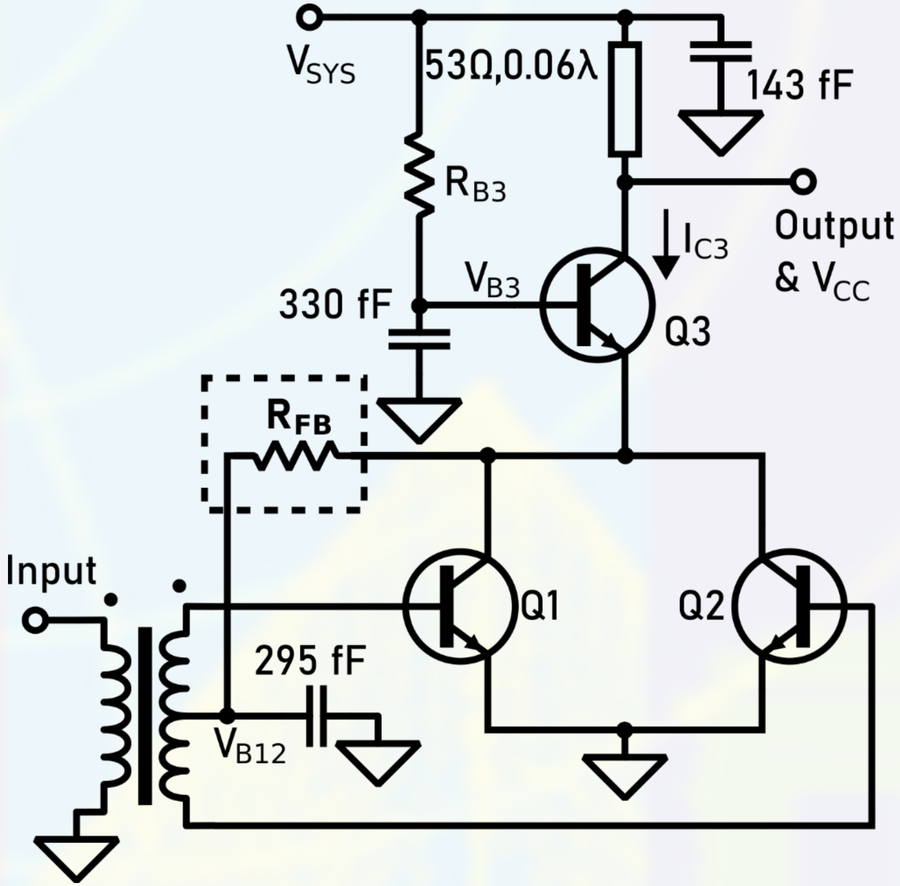


- ✅ Bias enforced with tail current source
- ✅ Gain maintained across input power
- ☠️ Higher power dissipation from current source with higher loss

U. Soylu, A. Alizadeh, M. Seo, and M. J. W. Rodwell, "280-GHz Frequency Multiplier Chains in 250-nm InP HBT Technology," *IEEE Journal of Solid-State Circuits*, vol. 58, no. 9, pp. 2421–2429, Sep. 2023, doi: 10.1109/JSSC.2023.3292182.

Proposed Design of This Work

- Q1/Q2: Main push-pull doubler
- Q3 provides
  - Amplification
  - Suppression of Miller Effect
  - Biasing
- **Feedback resistor R_{FB} adapts bias to resist additional current caused by input power changes**



Q1	2x6 um
Q2	2x6 um
Q3	2x6 um
R_{B3}	18.1 kΩ
R_{FB}	**18.1 kΩ**

V_{CC} V_{SYS}	3 V

I_{CC}	18.8 mA

DC Bias: Suppress Current Change

- Q1 and Q2 shorted at DC: treat as combined Q12
- Assumptions:

$$V_{B3} = V_{CC} - \frac{I_{C3}}{\beta_3} R_{B3} \qquad V_{BE3} \approx V_{BE12}$$

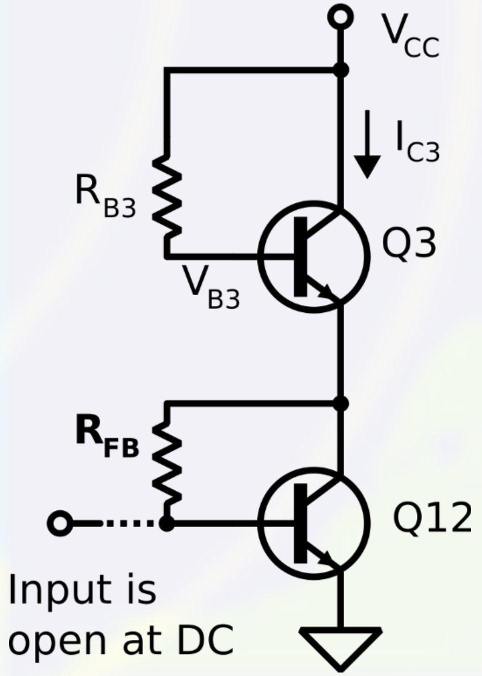
$$I_{C3} \approx I_{C12}$$

- Bias current is ultimately set by VCC, resistances, and β

$$I_{C3} = \beta_{12} \frac{V_{B3} - 2V_{BE}}{R_{FB}} = \frac{V_{CC} - 2V_{BE}}{R_{FB}/\beta_{12} + R_{B3}/\beta_3}$$

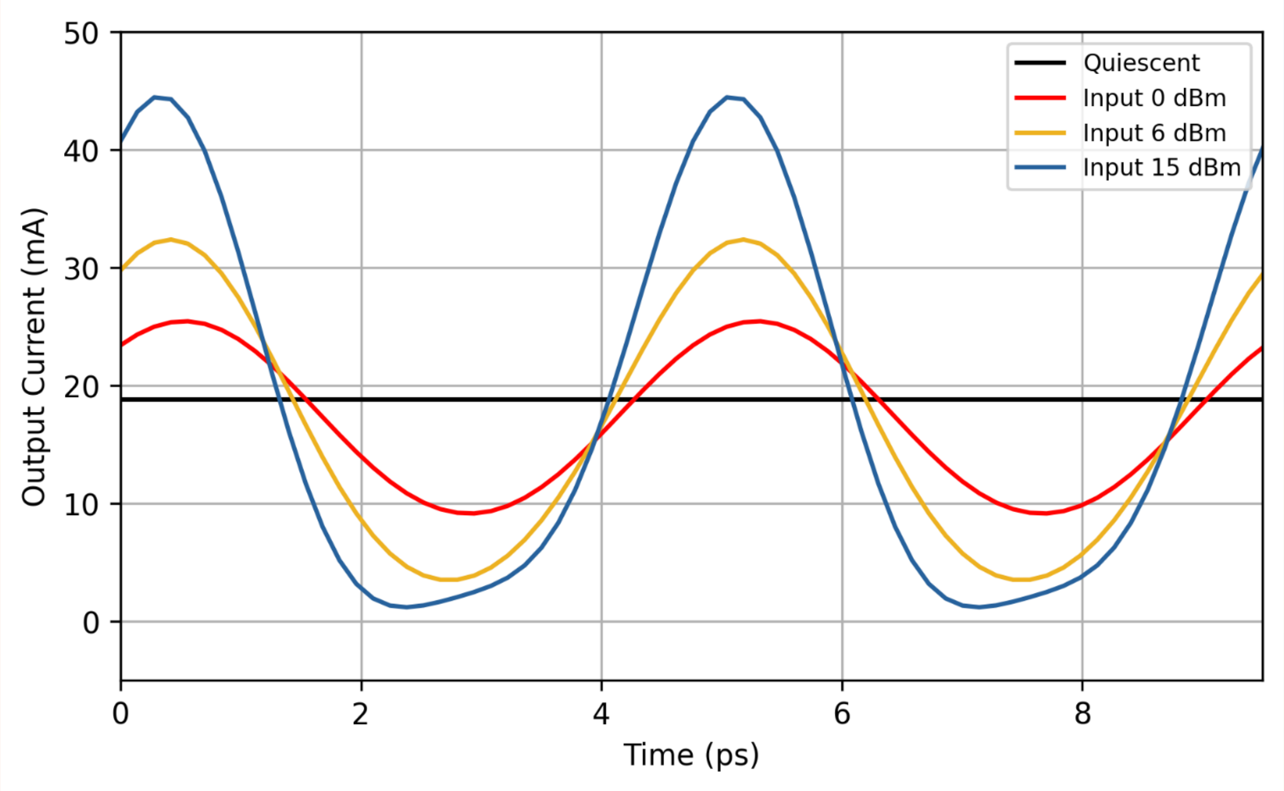
- **Current change suppressed by negative feedback on V_{BE}**

Equivalent DC Model



Effect of Feedback on DC Bias

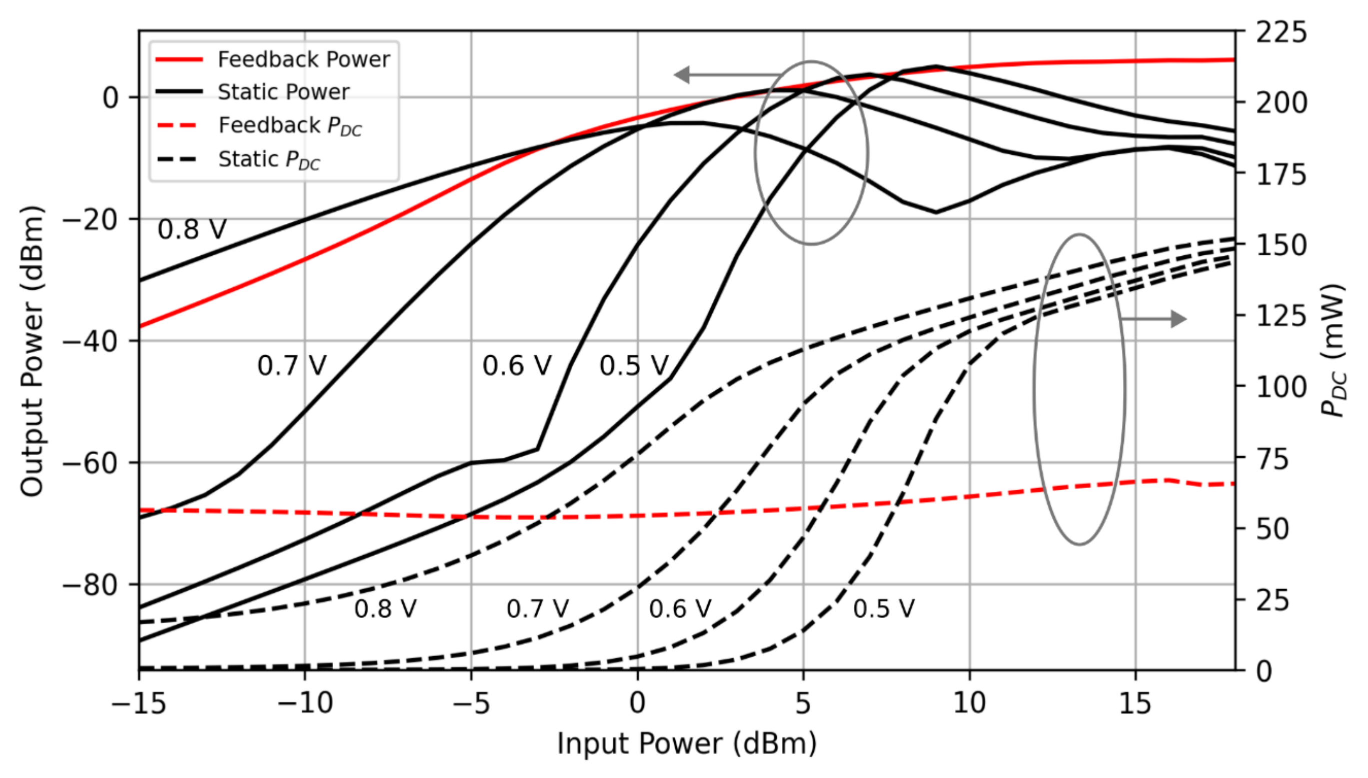
- DC bias is constant
- Transistor current density is maintained across power range



Simulated (Transistors only, no filtering)

Simulated Effect of Bias Feedback

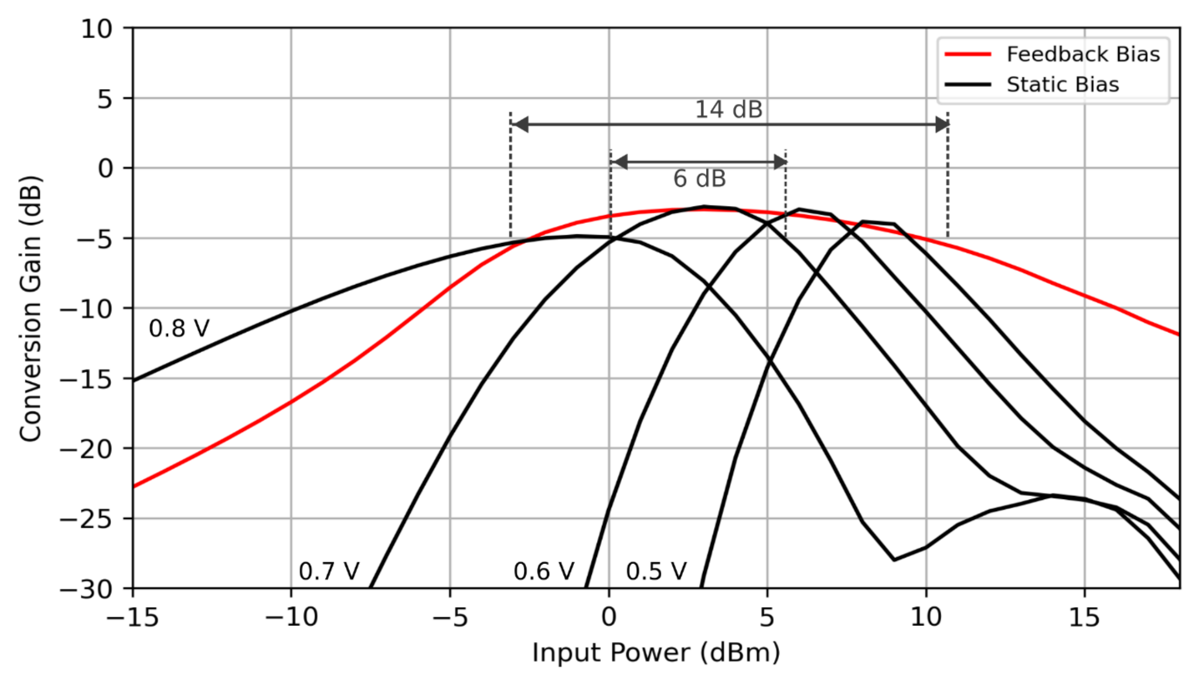
- Bias maintained across input powers
- ✅ Less gain sensitivity leading to control of output power
- ✅ Delivers same maximum output power as a tuned static bias for each input power



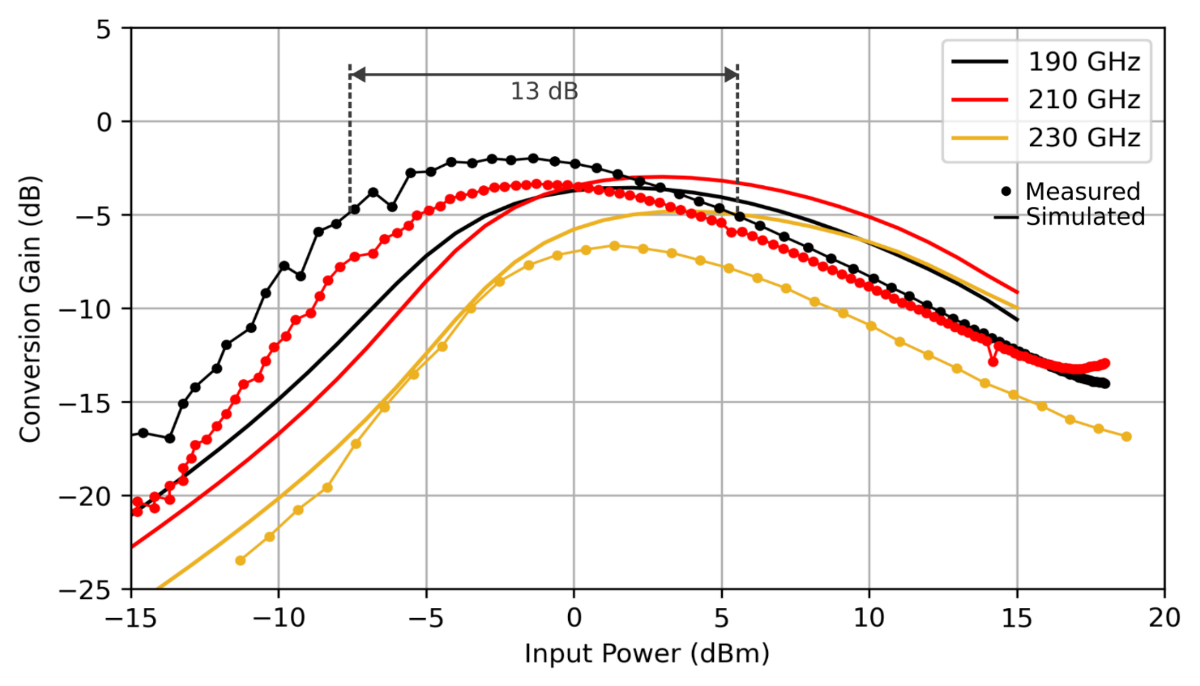
Measured Gain Over Input Power

- Adaptive bias feedback technique reduces input power sensitivity
- Demonstrated 13 dB input power range where gain is within 3 dB

Simulated Comparison: Static vs. Feedback Bias (210 GHz)



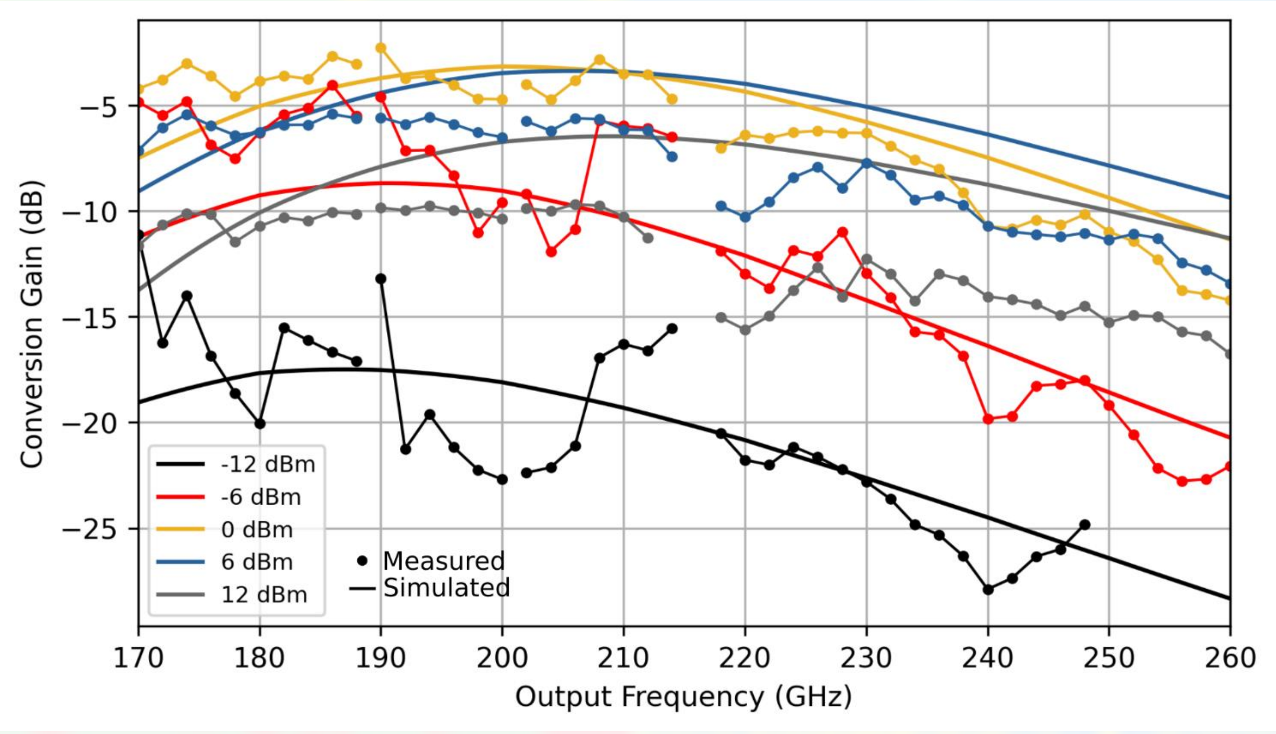
Measured Gain vs. Input Power



Measured Gain Across Frequency

- 3-dB bandwidth of 48 GHz
- Adaptive bias feedback works across frequency

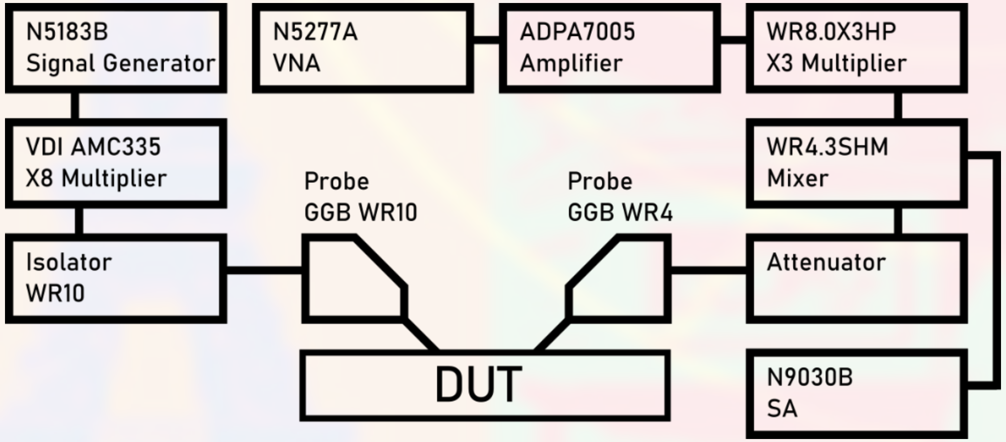
Measured Gain vs. Frequency for an Input Power



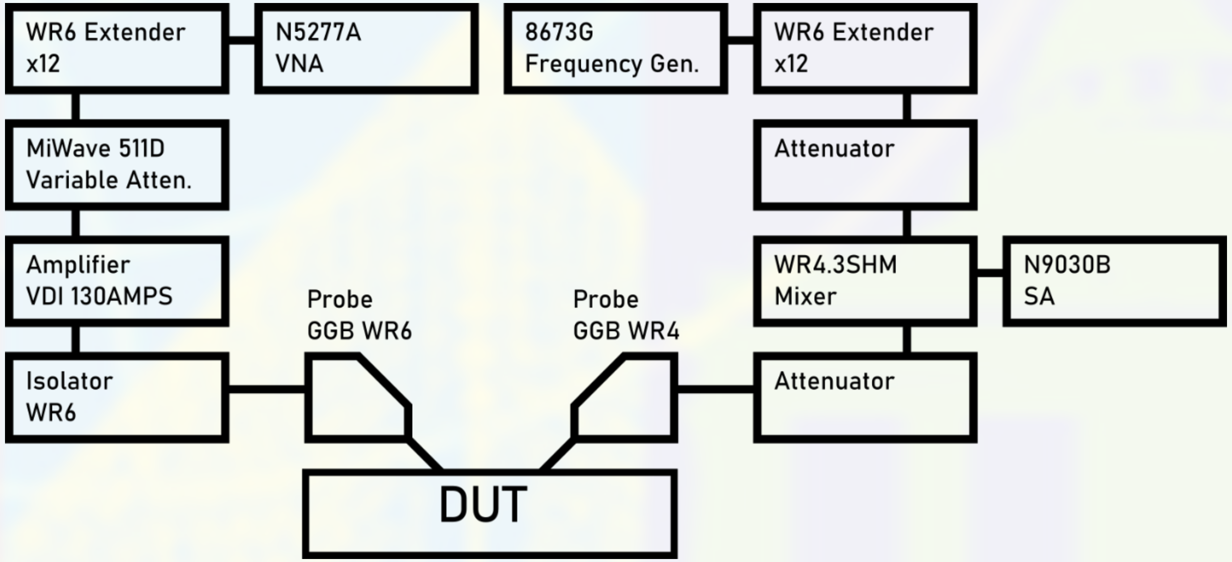
Measurement Setup

- Multiple setups used to cover entire frequency band

W-band Setup
Input: 75 GHz – 110 GHz
(Power controlled by signal generator power level)
Output: 170 GHz – 260 GHz

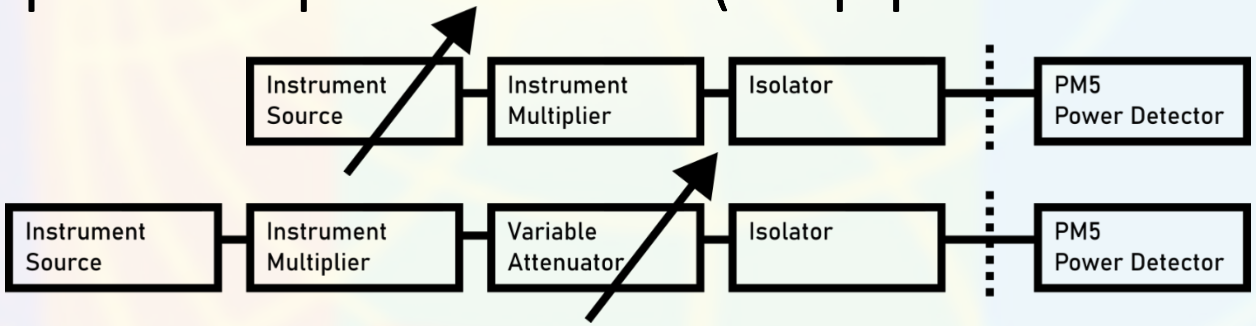


D-band Setup
Input: 110 GHz – 170 GHz
(Power controlled by variable attenuator)
Output: 170 GHz – 260 GHz



Measurement Setup: Calibration

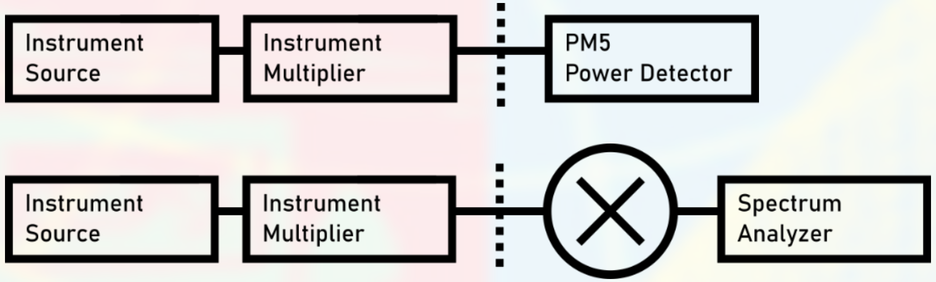
1. Input with power meter (Map power setting to input power)



W-band (75 GHz – 110 GHz)

D-band (110 GHz – 170 GHz)

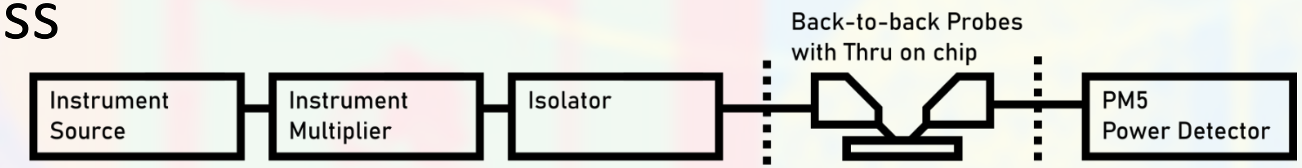
2. Down-conversion at output frequencies with spectrum analyzer



G-band (170 GHz – 260 GHz)

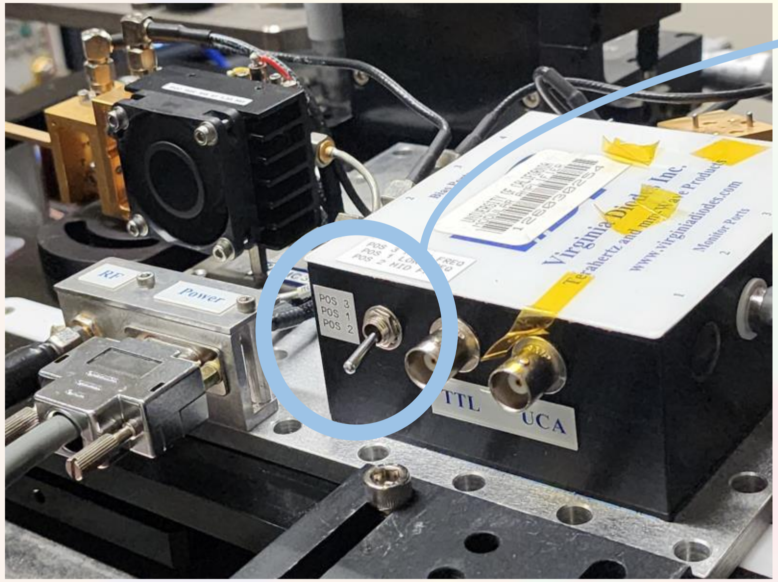
G-band (170 GHz – 260 GHz)

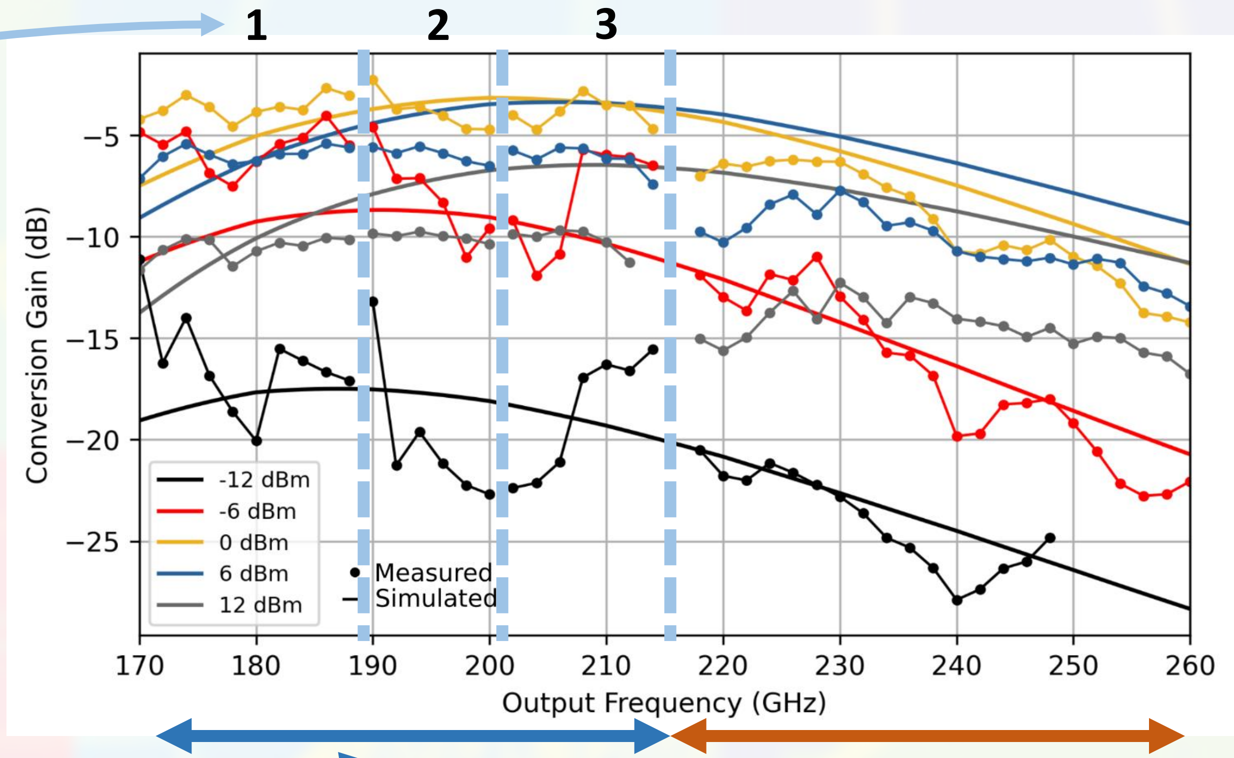
3. Probe loss



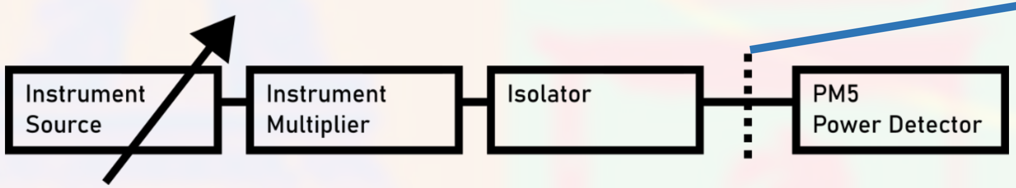
W-band, D-band, G-band

Measurement Setup: Ranges

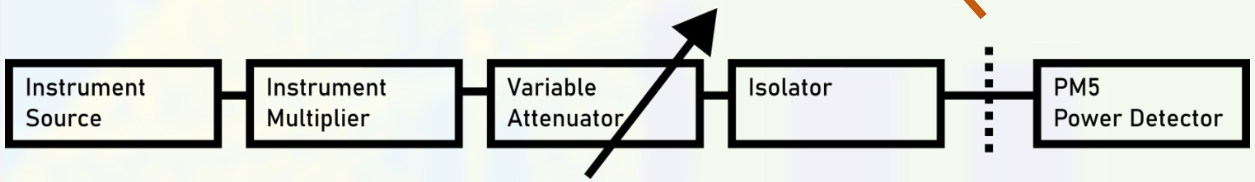




- Frequency gaps correspond to instrument ranges
- High instrument uncertainty when controlled with input power: **Instrument multiplier sensitivity**



W-band

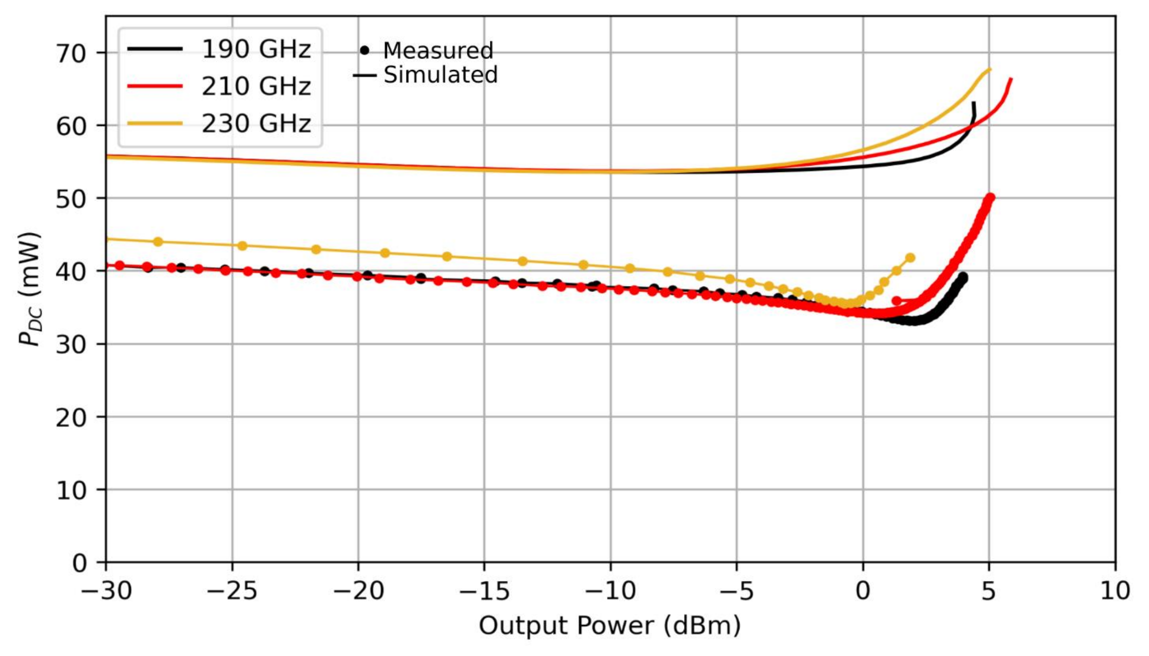


D-band

Feedback Maintains Bias

- Adaptive bias feedback eliminates additional DC current created by output waveform
- P_{DC} is held constant by feedback bias

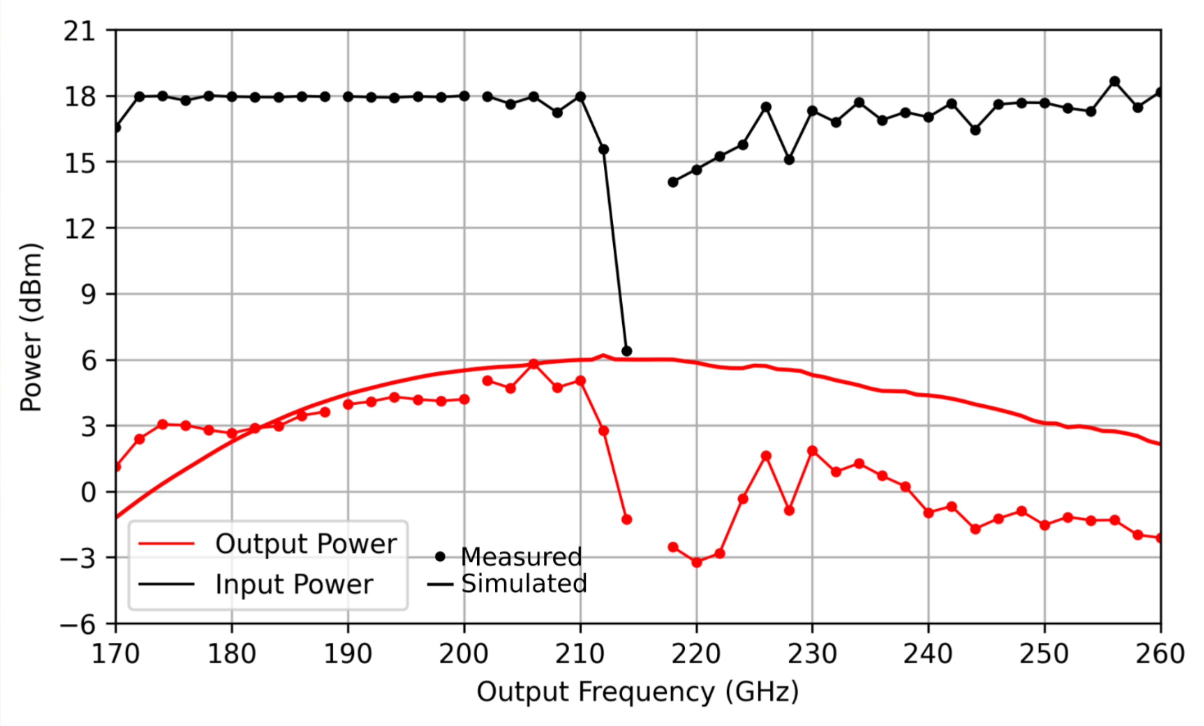
Measured Power Consumption vs. Output Power



Saturated Output Power

- Demonstrated > -3.3 dBm from 170 GHz to 260 GHz.
- Maximum 5.8 dBm at 206 GHz with 18 dBm of input power.

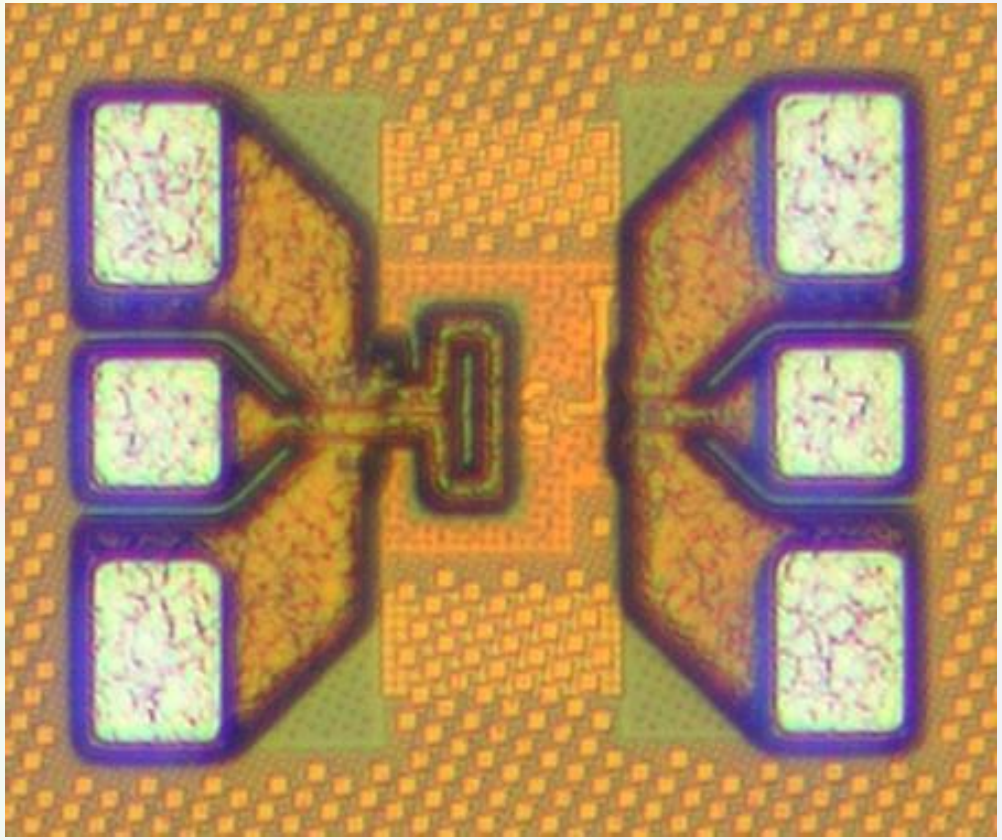
Highest Demonstrated Output Power with Instrument Input Power



This Work: G-band Doubler

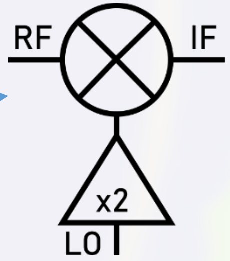
- **170-260 GHz SiGe Frequency Doubler with Adaptive Bias Feedback**
- 90-nm SiGe BiCMOS (Global Foundries 9HP+)

- Very compact!
  - 0.095 mm x 0.135 mm
    - Without pads



Comparison and Conclusion

- Adaptive bias feedback (one resistor) enables large input power range
  - No penalty to area, power consumption, or output power
- Enables dynamic system performance
  - Use varying LO power in an adaptive transceiver for different performance conditions



Ref.	This Work	[6]	[7]	[8]	[9]	[10]
Technology	90-nm SiGe BiCMOS	55-nm SiGe BiCMOS	130-nm SiGe BiCMOS	130-nm SiGe BiCMOS	90-nm SiGe BiCMOS	45-nm SOI CMOS
Type	Doubler + Amplifier	Doubler + Amplifier	Doubler + Amplifier	Doubler	Doubler	Doubler
Output Frequency (GHz)	206	245	152	204	228	150
BW_{3dB} (GHz)	170-218 ‡	220-260	138-170	165-230	200-245	135-160
Peak Gain (dB)	-2.0 §	10.9	4.9	-8.6	-15	-3
P_{sat} (dBm)	5.8	5.5	5.6	-2.6	2	3.5
P_{DC} (mW)	53	240	36	39	35	25
Efficiency (%)	7.2	9.5	10.9	1.4	4.5	9.0
Area (mm^2)	0.013†, 0.074	0.253	0.485	0.090	0.246	0.441
3-dB Gain Input Range (dB)	13.0 §	6 *	9 *	>7 *	>6 *	11 *

* Estimated from plot. † Area without pads. ‡ Lower end limited by G-band measurement, with 12 dBm input. § At 190 GHz.

Acknowledgements

- This work was supported by the Semiconductor Research Corporation (SRC) under the JUMP program, ComSenTer.
- The authors appreciate the support of GlobalFoundries for access to the 9HP process.
- The authors also thank Professor Gabriel Rebeiz for helping with the measurement.

Thanks!

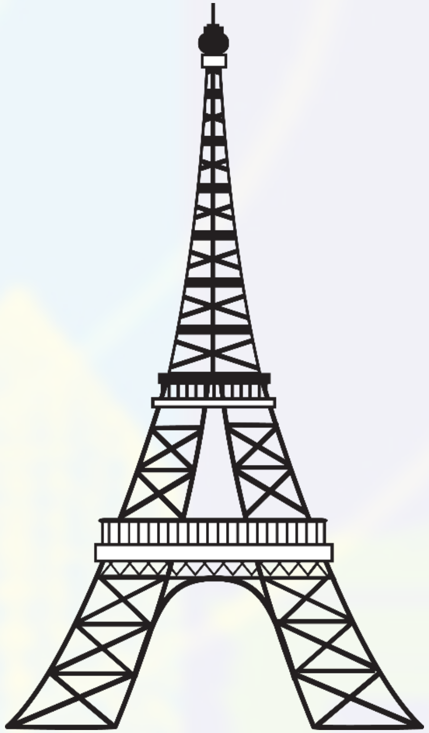


Table References

- [6] S. Shopov, A. Balteanu, J. Hasch, P. Chevalier, A. Cathelin, and S. P. Voinigescu, “A 234–261-GHz 55-nm SiGe BiCMOS Signal Source with 5.4–7.2 dBm Output Power, 1.3% DC-to-RF Efficiency, and 1-GHz Divided-Down Output,” IEEE Journal of Solid-State Circuits, vol. 51, no. 9, pp. 2054–2065, Sep. 2016, Conference Name: IEEE Journal of Solid-State Circuits, ISSN: 1558-173X. DOI: 10.1109/JSSC.2016.2560198.
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- [10] H.-C. Lin and G. M. Rebeiz, “A 135–160 GHz balanced frequency doubler in 45 nm CMOS with 3.5 dBm peak power,” in 2014 IEEE MTT-S International Microwave Symposium (IMS2014), ISSN: 0149-645X, Jun. 2014, pp. 1–4. DOI: 10.1109/MWSYM.2014.6848544.